

S/N TBD

Docket: CS01-150

Group art unit : ____ TBD

Date July 18, 2003

To: Commissioner of Patents and Trademarks
P.O. Box 1450 Alexandria, VA 22313-1450

Fr: William J. Stoffel Reg. No. 39,390 Cust No. 30402
PMB 455
1735 Market St - Suite A
Philadelphia, PA 19103

Subject:

Serial No. TDB
Docket CS1-150
File Date: with application
Inventor: Sheldon C. P. Lim

Title: A Method for Detecting and Monitoring Defects
Group art unit: TBD

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO A820 (also PTO-1449), Information
Disclosure Citation and references.

CERTIFICATE OF MAILING OR EXPRESS MAILING

I hereby certify that this correspondence is being deposited with the
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Signature/Date

William J. Stoffel 7/18/03
William J. Stoffel Reg. No. 39,390
Customer number 30402

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The following Patents and/or Publication are submitted to comply with the duty to disclose under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

US 6,403,389B1(Chang et al.) shows a method for measuring sheet resistance.

US 5,627,101(Lin et al.) shows a test method for a electro migration using a Metal and Poly test structure.

US 5,987,398(Halverson et al.) shows a method for SPC for a process having a non-constant mean of a response variable.

US 5,883,437(Maruyama et al.) discloses a method for applying a time varying voltage between the electrode and wiring pattern at different locations so as to detect a current flow and determine a defect by a variation in the detected current flow at the different locations and a portion of the defect.

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US 6,466,038 (Pekin, et al.) shows a method for non-isothermal electro migration testing of interconnects.

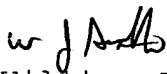
US 5,514,974 (Bouldin) shows a method for testing for metal failures by using 2 different test structures.

US 6,087,189 (Huang) shows test structure to monitor silicide.

US 5,552,718 (Bruce et al.) shows a test structure for space and line measurement.

Plusquellic et al., "Identification of defective CMOS devices using Correlation and Regression Analysis of Frequency Domain Transient Signal data", retrieved from website <http://www.csee.umbc.edu/~plusquel/pubs/itc97.pdf> on about May 20, 2003. No publication date listed.

Sincerely,



William J. Stoffel

Reg. No. 39,390

Customer number 30,402

Substitute for form 1449/PTO

(Use as many sheets as necessary)

Sheet 1 of 2

| | |
|------------------------|----------|
| Application Number | tbid |
| Filing Date | |
| First Named Inventor | Lim |
| Art Unit | |
| Examiner Name | |
| Attorney Docket Number | CS01-150 |

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Examiner
Signature

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| Date | |
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*EXAMINER: Initial # reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.¹ Applicant's unique citation designation number (optional).² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible.⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, Washington, DC 20231.**

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|---|------|--------------------------|---------|
| Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) | | Complete if Known | |
| | | Application Number | TBD |
| | | Filing Date | |
| | | First Named Inventor | Lim |
| | | Art Unit | |
| | | Examiner Name | |
| Sheet 2 | of 2 | Attorney Docket Number | cs01-50 |

| NON PATENT LITERATURE DOCUMENTS | | | |
|---------------------------------|-----------------------|---|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| | | PLUSQUELLIC et al., "Identification of defective CMOS devices using Correlation and Regression Analysis... Data" website www.CSEE, UMBC.edu | |
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| Examiner Signature | | Date Considered | |
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